Spintronics: The Future of Data Storage?

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Abstract

Reasearch and technology developments in the field of spintronics have grown tremendously in the past 10-15 years and already have had a major impact on the data storage industry. The future looks even brighter, as many new spintronic discoveries have been recently made that promise an even bigger impact in the future. This article summarizes the past accomplishments, describes some of the major discoveries that will have a lasting impact on the field, and discusses some of the technologies that may revolutionize data storage in the next decade.

Keywords: *magnetic, memory, spintronic.*

Introduction

The last 20 years have seen the emergence of significant new developments in magnetic data storage. The very rapid growth in magnetic disk drive capacity has been fueled by a series of discoveries and their rapid conversion into technology.

Giant Magnetoresistance

This article's starting point is the important discoveries in the late 1980s of giant magnetoresistance (GMR) in alternating magnetic–nonmagnetic multilayers independently by Fert[1] and Grunberg.[2] These discoveries were the first steps on the path toward the integration of spintronic devices into information technology. These early discoveries, however, were done at low temperatures and relatively high magnetic fields. It was not until the discoveries of GMR in Co/Cu multilayers at room temperature and low magnetic fields,[3] oscillatory interlayer coupling through Cu and other nonmagnetic noble and transition metals,[4] and interface engineering to create large GMR values in very small fields[5] that spintronics became a technological reality.

Spin Valve Technology

The first really significant technological discovery was the spin valve,[6] illustrated in Figure 1. This is a multilayer structure incorporating a "magnetically hard," or pinned, ferromagnetic layer on top (consisting of a bilayer of an antiferromagnet strongly coupled to a ferromagnetic layer), a nonmagnetic conductor layer (typically copper) in the middle, and a "magnetically soft," or "free," layer on the bottom just above the substrate. The pinning of the top ferromagnetic layer significantly biases the switching field for this layer far away from zero field, so it is not free to rotate at low fields. Thus, "pinning" means that this layer is always pointing in the same direction relative to the substrate. If the magnetic moments in the pinned and free layers are parallel, the current can flow easily throughout the structure, and the resistance is low. However, if the layers are magnetized oppositely, the current is impeded, and the resistance is high.

A spin valve can function as either a magnetic field sensor or a hysteretic memory device, depending on how easy it is to rotate the moment of the free layer from parallel to antiparallel with respect to the pinned layer. In the early 1990s, IBM started a project to develop such GMR devices as read-head sensors for magnetic disk drives and introduced them to the marketplace in 1998. This introduction had an almost immediate impact on disk drive capacity that has lasted to the present day.

Magnetic Random-Access Memory (MRAM)

Concurrent with the development of the read-head sensor at IBM, the Defense Advanced Research Projects Agency (DARPA) funded the GMR Consortium—which included Honeywell, Nonvolatile Electronics Inc., Federal Products, the Naval Research Laboratory, and HRL (formerly Hughes Research Laboratory)—to explore various other potential applications that it believed would have a significant impact on Department of Defense (DoD) systems. One of the major motivations for this project was a strong DoD need for a nonvolatile, radiation-hard, random-access memory to replace current memories that were very bulky (40 lb for 128 kbit) and expensive. One of the major outcomes of this consortium was the realization that the development of such a memory not only was possible but also could provide an important new universal nonvolatile memory with the density of DRAM (dynamic random-access memory), the speed of SRAM (static random-access memory), unlimited write cycles, and significantly lower write-power requirements than flash memory (commonly used in memory sticks, digital cameras, and cell phones).

With this realization, DARPA initiated a project to develop magnetoresistive memories and complementary sensors that soon was named the Spintronics (spin transport electronics) Project. This project, started in 1996, culminated with the development of a truly revolutionary magnetic random-access memory (MRAM) by both Motorola (and subsequently by Freescale, which was spun out of Motorola as a subsidiary and then became an independent company) and IBM. In fact, the magnetoresistive device developed by Motorola and IBM was a spin-valve–like component in which the nonmagnetic metal was replaced by a very thin (1.2 nm) insulating layer that formed

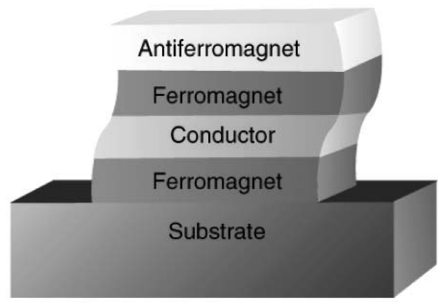

Figure 1. Basic heterostructure of a spin valve. See text for details.

a tunnel junction between the ferromagnetic layers. The virtue of this magnetic tunnel junction[7] was a much larger change in resistance from the parallel to the antiparallel magnetization states; this resistance was a closer match to the circuit requirements.

The road to the development of MRAM had many twists and turns and is summarized in several very fine technical articles[8–10] and in Figure 2, which shows several milestone MRAM chips that chronicle the progress over the years.

Challenges for Fully Scalable MRAM

Toggle Switching

Although remarkable progress has been made in the last decade, the pathway to a fully scalable MRAM requires some significant innovations. One recent discovery, already in use by Freescale and IBM, is a novel method for switching the magnetization in the free layer.[11]

In this approach, the free layer is actually an artificial ferromagnet consisting of two ferromagnetic layers separated by a very thin ruthenium layer. The two ferromagnetic layers are antiferromagnetically coupled. The bottom film forms the top electrode of a tunnel junction, and the resistance of the tunnel junction is determined by the direction of the magnetization of this film. This slightly elliptical "bit" is oriented at 45° to the two current leads (the bit line and the word line), which are two leads at 90° to one another that are used to produce the rotating field that is used to switch the bit. Current in the bit line "scissors" the magnetization in the two ferromagnetic layers of the antiferromagnet, providing a small magnetization perpendicular to their original direction. Current in the word line then toggles the magnetization, reversing the directions of both layers of the artificial antiferromagnet; more importantly, it reverses the direction of the magnetization of the layer on top of the tunnel barrier, dramatically changing the resistance of the tunnel junction.

This toggle method of switching is illustrated in Figure 3. Toggle switching solves the "half select" error sometimes seen in the conventional switching method in which a bit changes its status when only half the necessary current is flowing—either from the bit line or the word line. This occurs because the free layer is a single ferromag-

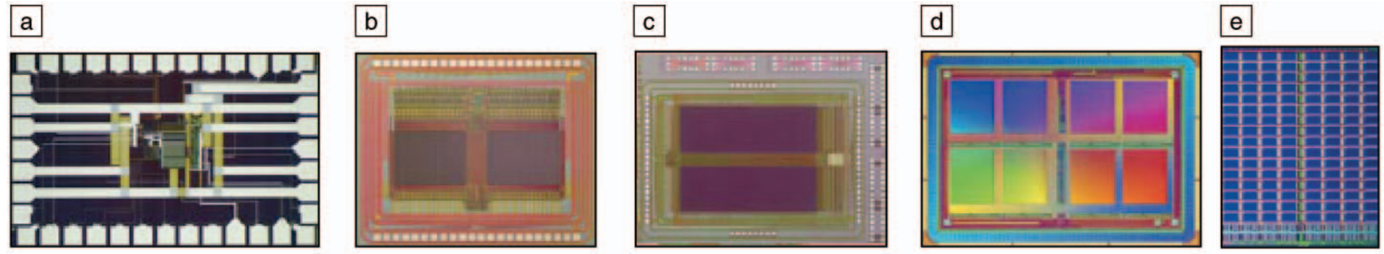

Figure 2. Photomicrographs showing the increasing density of prototype magnetic random-access memory (MRAM) chips. (a) IBM 1 mm × 1.5 mm, 1 kbit chip with a 5.4-μm² twin cell in 0.25-μm technology with approximately 3–10-ns access time (from Reference 22, with permission). (b) Motorola 3.9 mm × 3.2 mm, 256 kbit chip with 7.1-μm² cell in 0.6-μm technology with 50-ns access time (from Reference 23, with permission). (c) Motorola 4.25 mm × 5.89 mm, 1 Mbit chip with 7.1-μm² cell in 0.6-μm technology with 50-ns access time (from Reference 24, with permission). (d) Motorola 4.5 mm × 6.3 mm, 4 Mbit chip with 1.55-μm² cell in 180-nm technology with 25-ns access time (from Reference 17, with permission). (e) IBM 7.9 mm × 10 mm, 16 Mbit chip with 1.42-μm² cell in 180-nm technology with 30-ns access time (adapted from Reference 21, with permission).

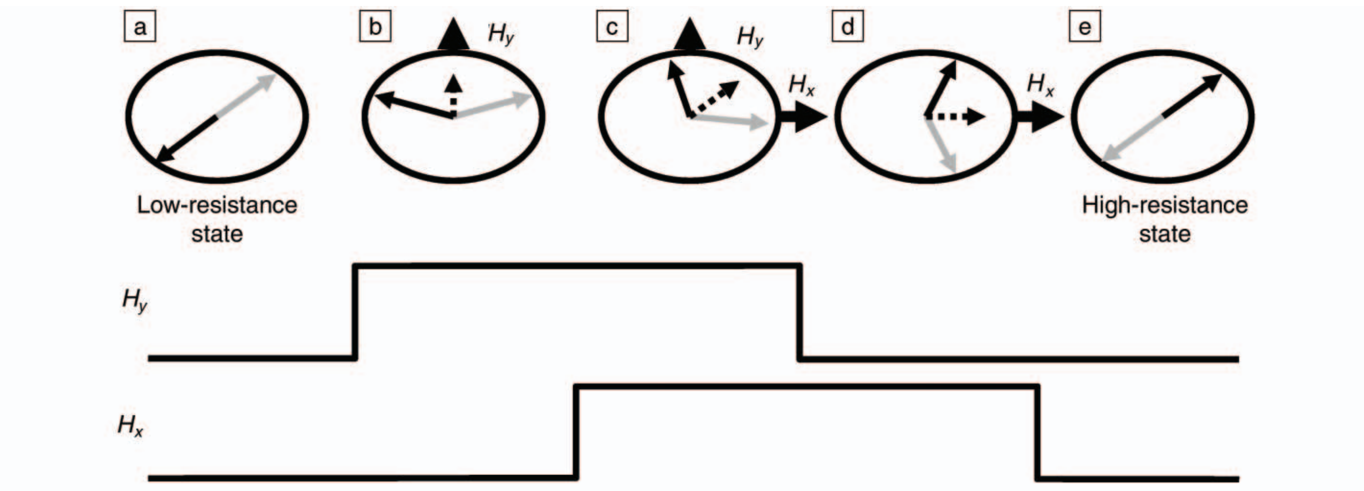

Figure 3. Schematic illustration of the operation of the toggling method of MRAM switching. Dark arrows represent the direction of magnetization of the film just above the tunnel barrier and determine the magnetoresistance of the tunnel junction. (a) Initial state of the structure (low resistance when the magnetization of the lower ferromagnet is aligned with the pinned layer on the other side of the tunnel barrier). (b) Current in the bit line is turned on, producing a field in the y-direction (H_y), as illustrated by the upper square wave in the lower part of the figure; the magnetizations of both layers rotate and "scissor," producing a net moment in the y-direction. (c) Current in the word line is turned on (lower square wave in the figure), producing a field in the x-direction (H_x); the two layers scissor more and the direction of the net moment is rotated towards the x-direction. (d) When the bit line current is turned off, the net moment rotates to be aligned with the x-axis. (e) Finally, when the word line current is turned off, the layers have "toggled" a full 180°.

netic layer.[12] In the toggle device, neither the bit nor word current by itself will cause the bit to change status.

Another benefit of toggle switching lies in the properties of the artificial antiferromagnet. In order for this bit to be stable as its dimensions shrink, the anisotropy energy must be a factor of 30–50 larger than kT. If the volume gets smaller, the magnetic anisotropy must be increased. The magnetic anisotropy of this and similar composite structures can be more easily controlled than that of a single layer, allowing the bit to scale to dimensions smaller than the conventional MRAM bit.[12]

Recently, magnetic tunnel junctions were significantly improved with the discovery of much higher magnetoresistive ratios using magnesium oxide tunnel barriers instead of the aluminum oxide barriers that are used in the current MRAM demonstrations (see also the article by Parkin in this issue). These new junctions have magnetoresistive ratios of several hundred percent, compared with values of less than 100% for aluminum oxide.[13]

Spin Momentum Transfer

Another key development that will allow further scaling of MRAM is the demonstration of nanoscale-current-driven magnetization reversal in trilayer GMR structures similar to those shown in Figure 1.[14] This development is key for scaling MRAM to at least the 32-nm lithography node and probably beyond. The 32-nm node is a few generations from the 65-nm node currently being introduced. This novel spin momentum transfer (SMT) effect involving nanoscale-current-driven magnetization reversal was predicted in 1996 by Slonczewski and Berger[15,16] but not experimentally realized until 2000 with a key demonstration by Katine et al. in nanoscale trilayers.[14] SMT switching does not require the generation of magnetic fields to rotate the magnetization; it just requires current to flow through the structure.

The only requirement for SMT switching is that the largest dimension of the bit must be well under 100 nm. Not only will this innovation significantly shrink the size of the bit by reducing the number of leads, but we project that this will allow the bit to be switched at a much lower energy than the "conventional" or the "toggle" bit, provided that we can get close to the theoretical limit for the switching currents (1–2 orders of magnitude lower than what has been demonstrated to date). Based on what we feel are reasonable assumptions about the currents required for SMT switching, we have projected the key features of the future MRAM incorporating SMT switching in Table I. We have also listed in the table the features of current semiconducting random-access memories including DRAM and SRAM, which are volatile memories, and flash memory, which is nonvolatile but has a limited number of write cycles.

Domain Walls for Mass Memory Storage

This is certainly not the end of the story. There is perhaps an even more interesting development based to a large extent on SMT. This effect can also be used to move domain walls in soft magnetic structures, and based on this novel idea, Parkin has proposed a new, all-solid-state archival storage that rivals the density of magnetic disk drives but with no moving parts and which can be completely processed using more or less conventional semiconductor fabrication.[17] This memory stores information as domain walls in a nanoscale magnetic film deposited in a deep trench on a silicon chip, similar to the trenches used for DRAM. Ones and zeros are marked by the presence or absence of a domain wall at precise locations on the film that in the trench resemble a racetrack. There are several key features of domain walls that are utilized in the memory. A domain wall has a very large fringing field that can be used to create a domain wall in a neighboring film. This is the key to the writing of this memory. A domain wall in a separate magnetic layer closely coupled to the storage layer can be moved closer or further away from its neighbor using a small SMT current. If the writing domain wall is close to the storage layer, it creates a wall writing a one. If it is further away, then there is no domain wall created, (i.e., a zero). The domain wall in the storage layer can be shuttled around using an SMT current passed through the storage layer. The ones and zeros are read by a small magnetic tunnel junction located adjacent to the writing film. The domain walls are moved by the read head, just as the bits on a hard disk are moved past the read head. However, in this case the movement is strictly magnetic, not mechanical. This novel structure is illustrated in Figure 4.

This mass storage memory has the potential to store at least 100 bits in the space of one DRAM bit, providing densities that definitely will rival hard disk drives and have the potential for low-cost manufacturing. So, as mechanical drives reach their density limits in the next decade, a pathway exists to provide ever-increasing densities for mass storage.

Table I: Projected Performance of MRAM, SMT MRAM, and Conventional Semiconducting Memories.

	Standard MRAM (90 nm)[a]	DRAM (90 nm)[b]	SRAM (90 nm)[b]	SMT MRAM (90 nm)[a]	Flash (90 nm)[b]	Flash (32 nm)[b]	SMT MRAM (32 nm)[a]
Cell Size (μm^2)	0.25	0.25	1–1.3	0.12	0.1	0.02	0.01
	256 Mbit/cm	256 Mbit/cm	64 Mbit/cm	512 Mbit/cm	512 Mbit/cm	2.5 Gbit/cm	5 Gbit/cm
Read Time	10 ns	10 ns	1.1 ns	10 ns	10–50 ns	10–50 ns	1 ns
Program Time	5–20 ns	10 ns	1.1 ns	10 ns	0.1–100 ms	0.1–100 ms	1 ns
Program Energy/Bit	120 pJ	5 pJ	5 pJ	0.4 pJ	30–120 nJ	10 nJ	0.02 pJ
	Needs refresh						
Endurance	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$ read, $>10^{6}$ write	$>10^{15}$ read, $>10^{6}$ write	$>10^{15}$
Nonvolatility	Yes	No	No	Yes	Yes	Yes	Yes

Notes: MRAM = magnetic random-access memory. SMT = spin momentum transfer. DRAM = dynamic random-access memory. SRAM = static random-access memory.
[a] MRAM values as projected by the authors.
[b] These values are from the International Technology Roadmap for Semiconductors.

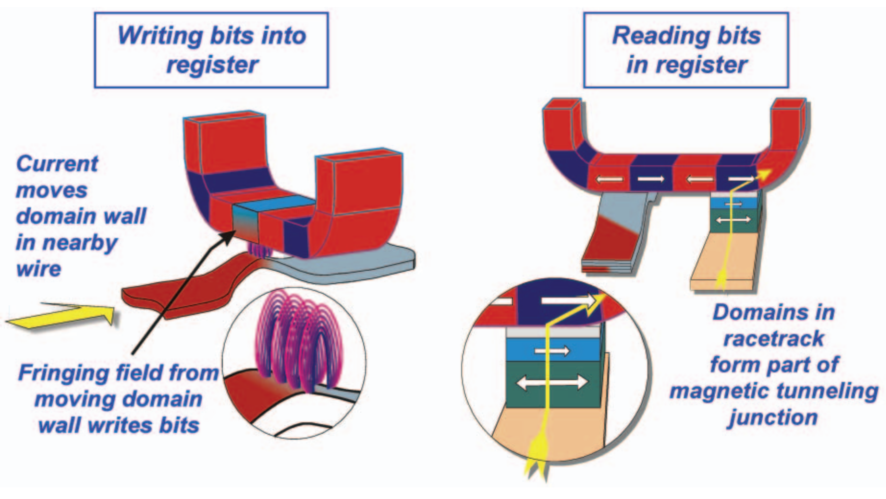

Figure 4. Key features of the "racetrack" memory. See text for details.

Summary

We hope it is clear that spintronics will play a key role in the future of data storage for both random-access and mass storage. If all the developments that are described in this short review come to fruition, indeed spintronics could well be the future of data storage.

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